GENERAL DESCRIPTION

Passivated guaranteed commutation triacs in a plastic envelope intended for use in motor control circuits or with other highly inductive loads. These devices balance the requirements of commutation performance and gate sensitivity. The "sensitive gate" E series and "logic level" D series are intended for interfacing with low power drivers, including micro controllers.

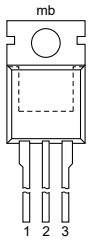
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
	BTA216-	**600D**	
	BTA216-	**600E**	
	BTA216-	**600F**	
V_{DRM}	Repetitive peak off-state voltages	600	V
$I_{T(RMS)}$	RMS on-state current	16	A
I_{TSM}	Non-repetitive peak on-state current	140	A

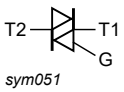
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DRM}	Repetitive peak off-state voltages		-	600[1]	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 99$ ˚C	-	16	A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 25$ ˚C prior to surge			
		t = 20 ms	-	140	A
		t = 16.7 ms	-	150	A
I^2t	I^2t for fusing	t = 10 ms	-	98	A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs	-	100	A/µs
I_{GM}	Peak gate current		-	2	A
P_{GM}	Peak gate power		-	5	W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5	W
T_{stg}	Storage temperature		-40	150	˚C
T_j	Operating junction temperature		-	125	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	1.2	K/W
		half cycle	-	-	1.7	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
		BTA216-		...D	...E	...F	
I_{GT}	Gate trigger current[2]	V_D = 12 V; I_T = 0.1 A					
		T2+ G+	-	5	10	25	mA
		T2+ G-	-	5	10	25	mA
		T2- G-	-	5	10	25	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A					
		T2+ G+	-	15	25	30	mA
		T2+ G-	-	25	30	40	mA
		T2- G-	-	25	30	40	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	15	25	30	mA
			...D, E, F				
V_T	On-state voltage	I_T = 20 A	-	1.5			V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	1.5			V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	-			V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.5			mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.			MAX.	UNIT
		BTA216-	...D	...E	...F		
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 110 ˚C; exponential waveform; gate open circuit	30	60	70	-	V/µs
dI_{com}/dt	Critical rate of change of commutating current	V_{DM} = 400 V; T_j = 125 ˚C; $I_{T(RMS)}$ = 16 A; dV_{com}/dt = 10V/µs; gate open circuit	2.5	6.2	18	-	A/ms
dI_{com}/dt	Critical rate of change of commutating current	V_{DM} = 400 V; T_j = 125 ˚C; $I_{T(RMS)}$ = 16 A; dV_{com}/dt = 0.1V/µs; gate open circuit	12	20	50	-	A/ms

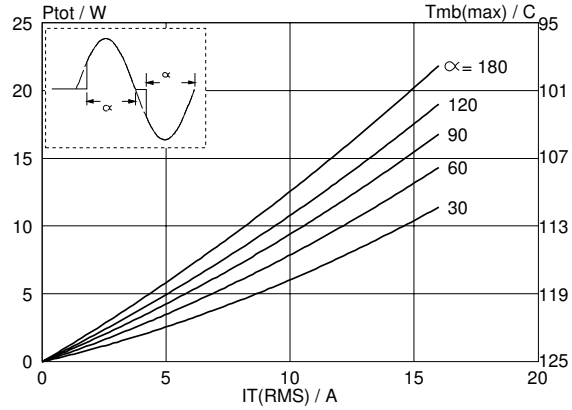


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

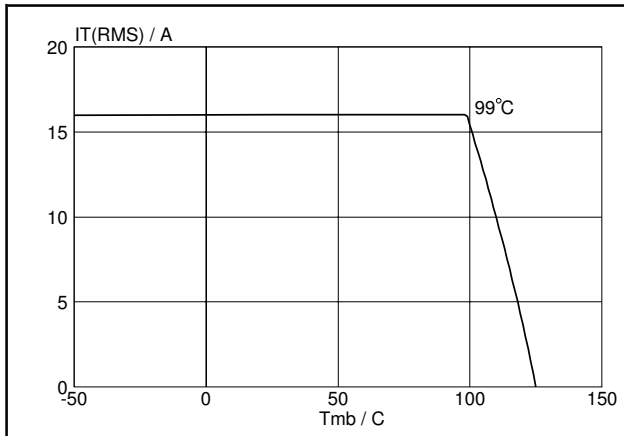


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

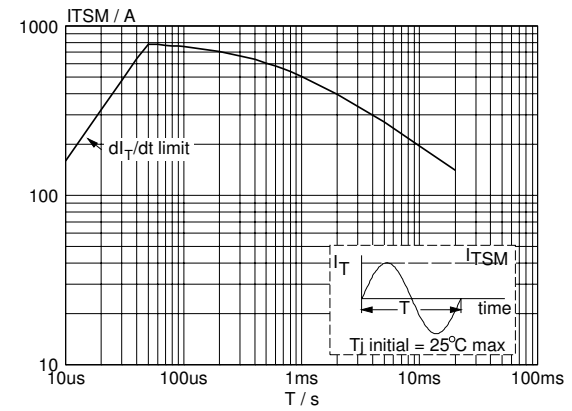


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

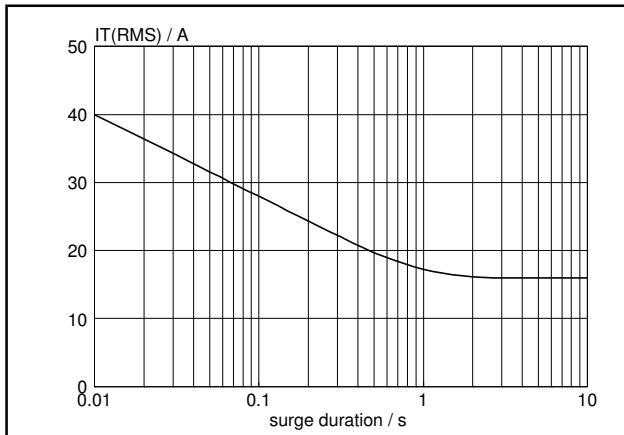


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99˚C$.

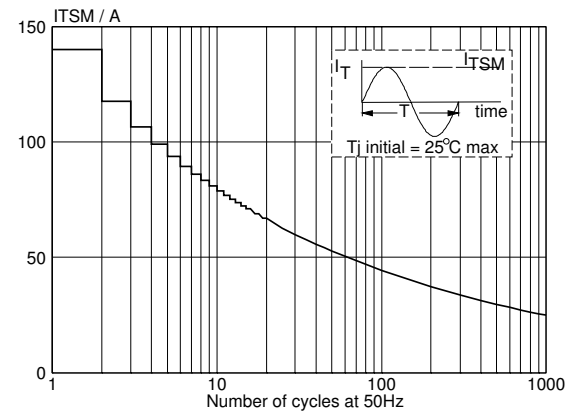


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

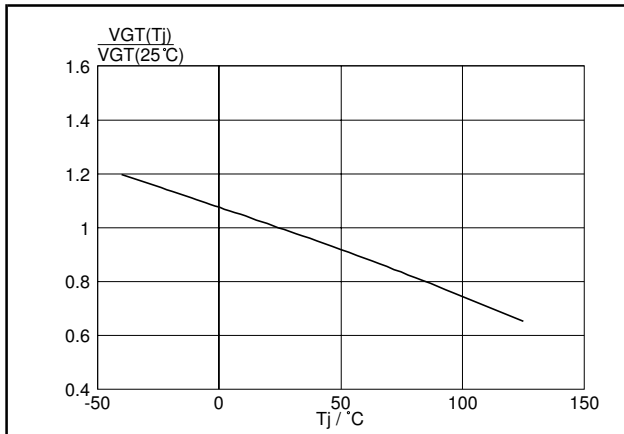


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25˚C)$, versus junction temperature T_j.

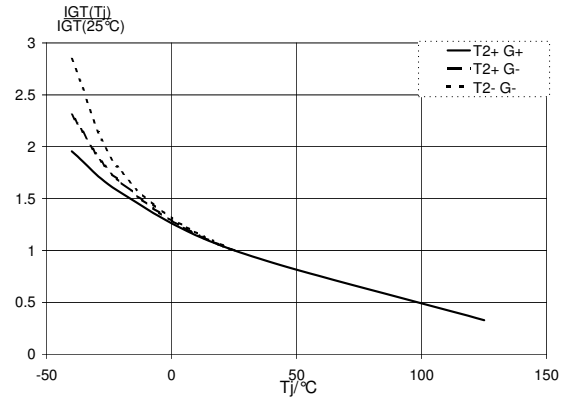


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25^{\circ}C)$, versus junction temperature T_j.

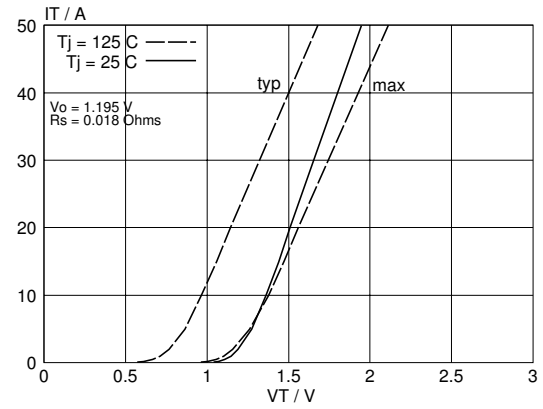


Fig.10. Typical and maximum on-state characteristic.

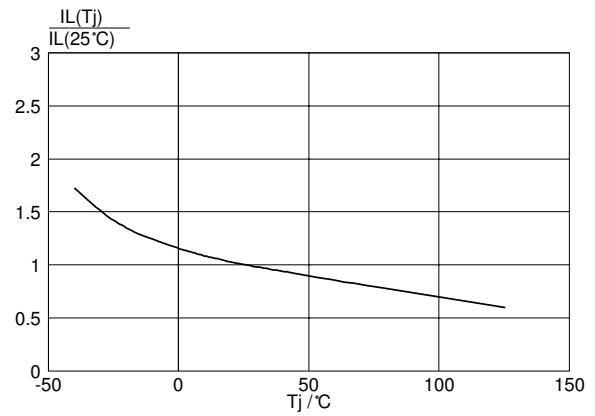


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25^{\circ}C)$, versus junction temperature T_j.

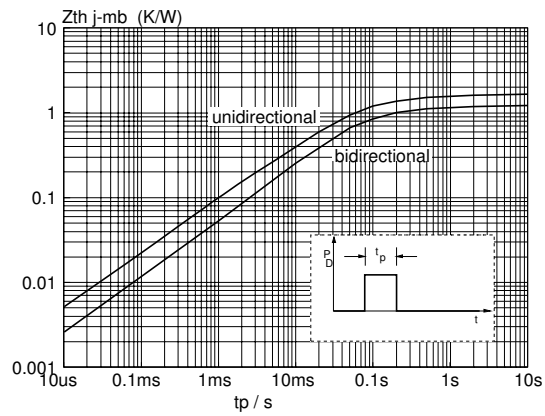


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

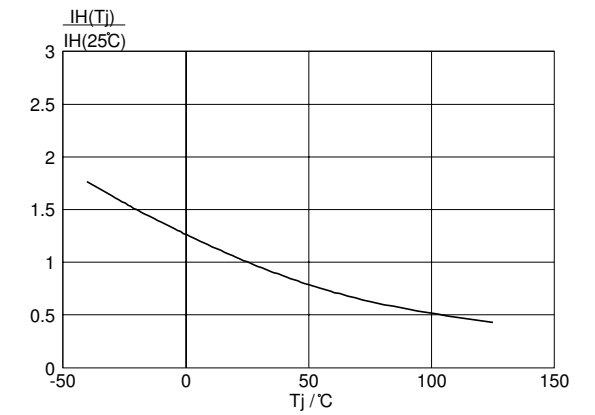


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25^{\circ}C)$, versus junction temperature T_j.

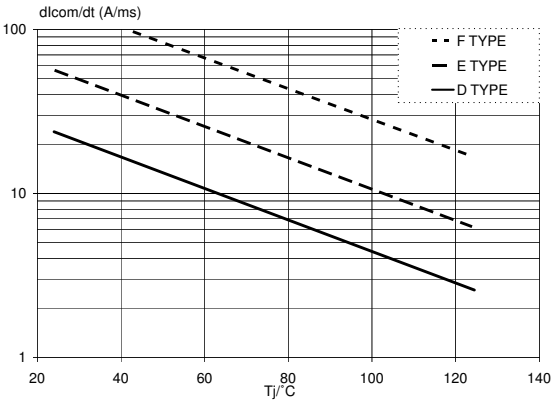
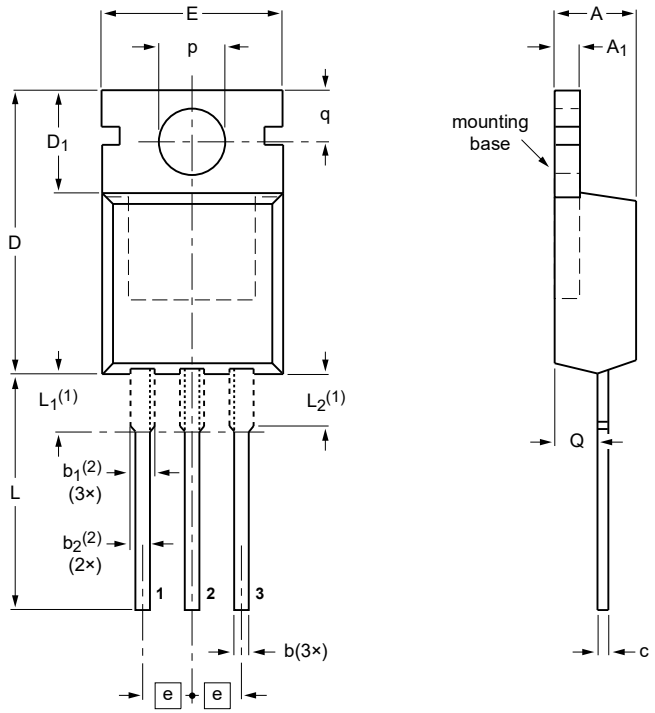


Fig.12. Minimum, critical rate of change of commutating current dI_{com}/dt versus junction temperature, dV_{com}/dt = 10V/µs.

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1(2)	b_2(2)	c	D	D_1	E	e	L	L_1(1)	L_2(1) max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

Notes
1. Lead shoulder designs may vary.
2. Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78		3-lead TO-220AB	SC-46			~~08-04-23~~ 08-06-13