1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT186A (TO-220F) "full pack" plastic package intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance.

2. Features and benefits

- High bidirectional blocking voltage capability
- High thermal cycling performance
- Isolated mounting base package
- Planar passivated for voltage ruggedness and reliability

3. Applications

- Capacitive Discharge Ignition (CDI)
- Crowbar protection
- Inrush protection
- Motor control
- Voltage regulation

4. Quick reference data

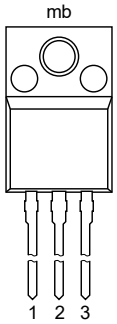
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RRM}	repetitive peak reverse voltage			-	-	800	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_h \leq 69$ °C		-	-	7.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_h \leq 69$ °C; Fig. 1; Fig. 2; Fig. 3		-	-	12	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5		-	-	100	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms		-	-	120	A
T_j	junction temperature			-	-	125	°C
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12$ V; $I_T = 0.1$ A; $T_j = 25$ °C; Fig. 7		-	2	15	mA
Dynamic characteristics							

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; R_{GK} = 100 Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 12		200	1000	-	V/µs
		V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 12		50	130	-	V/µs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 TO-220F (SOT186A)	
2	A	anode		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT151X-800C	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
V_{RRM}	repetitive peak reverse voltage			-	800	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_h \leq$ 69 °C		-	7.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_h \leq$ 69 °C; Fig. 1; Fig. 2; Fig. 3		-	12	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	100	A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms		-	120	A
I^2t	I^2t for fusing	t_p = 10 ms; SIN		-	50	A^2s
dI_T/dt	rate of rise of on-state current	I_G = 30 mA		-	50	A/µs
I_{GM}	peak gate current			-	2	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C

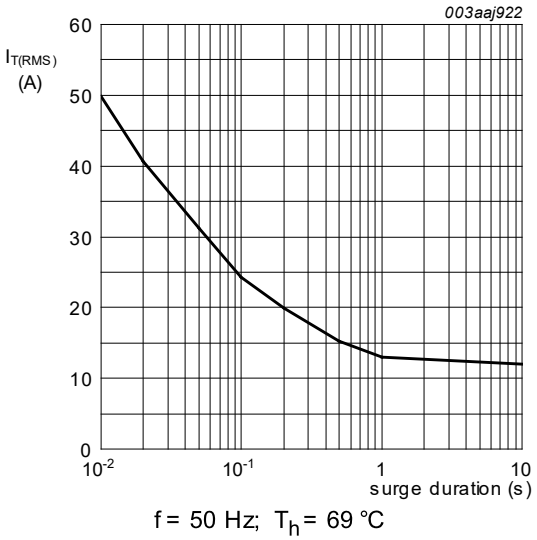


Fig. 1. RMS on-state current as a function of surge duration; maximum values

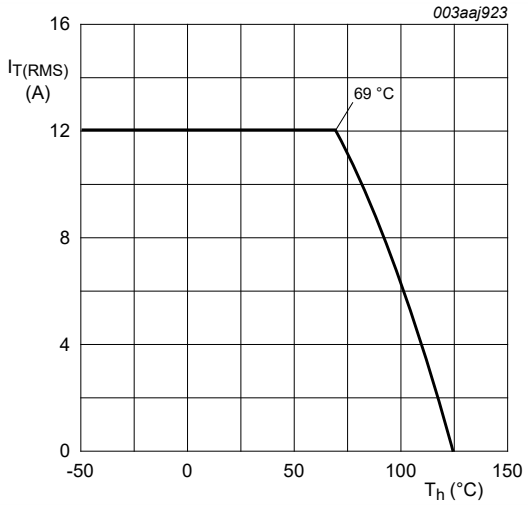
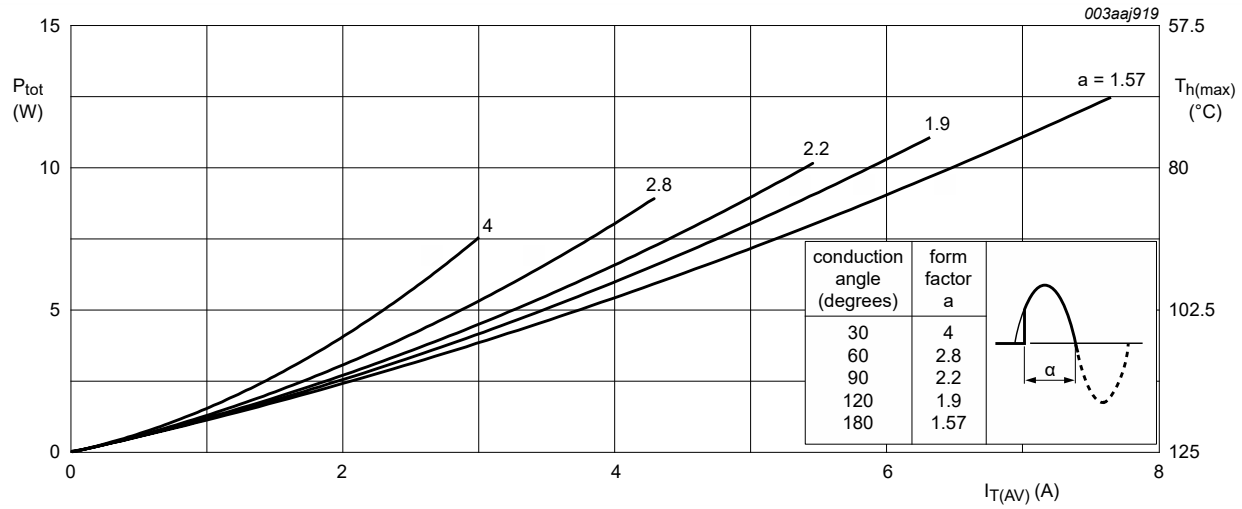
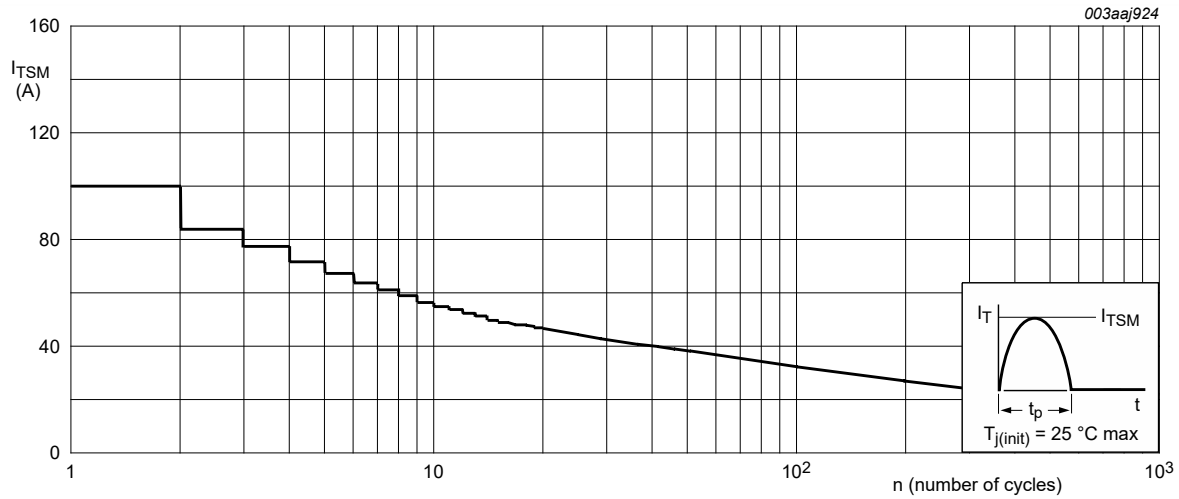


Fig. 2. RMS on-state current as a function of heatsink temperature; maximum values



α = conduction angle a = form factor = $I_{T(RMS)} / I_{T(AV)}$

Fig. 3. Total power dissipation as a function of average on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 7		-	2	15	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T_j = 25 °C; Fig. 8		-	10	40	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	7	20	mA
V_T	on-state voltage	I_T = 23 A; T_j = 25 °C; Fig. 10		-	1.4	1.75	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 11		-	0.6	1	V
		V_D = 800 V; I_T = 0.1 A; T_j = 125 °C; Fig. 11		0.25	0.4	-	V
I_D	off-state current	V_D = 800 V; T_j = 125 °C		-	0.1	0.5	mA
I_R	reverse current	V_R = 800 V; T_j = 125 °C		-	0.1	0.5	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; R_{GK} = 100 Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 12		200	1000	-	V/µs
		V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 12		50	130	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 40 A; V_D = 800 V; I_G = 100 mA; dI_G/dt = 5 A/µs; T_j = 25 °C		-	2	-	µs
t_q	commutated turn-off time	V_{DM} = 536 V; T_j = 125 °C; I_{TM} = 20 A; V_R = 25 V; $(dI_T/dt)_M$ = 30 A/µs; dV_D/dt = 50 V/µs; $R_{GK(ext)}$ = 100 Ω; (V_{DM} = 67% of V_{DRM})		-	70	-	µs

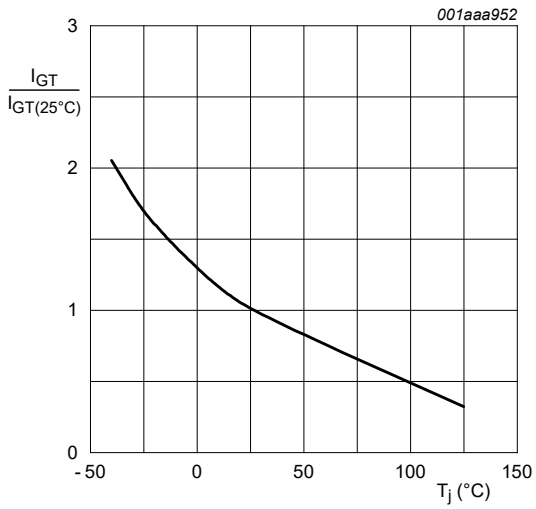


Fig. 7. Normalized gate trigger current as a function of junction temperature

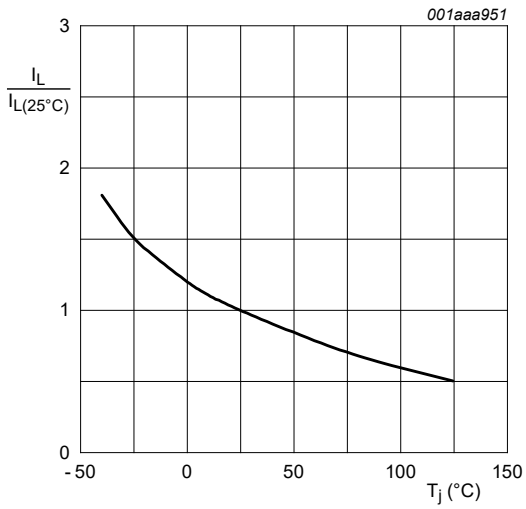


Fig. 8. Normalized latching current as a function of junction temperature

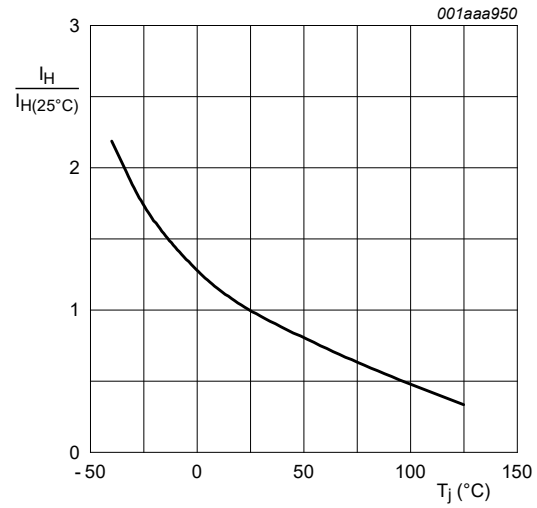
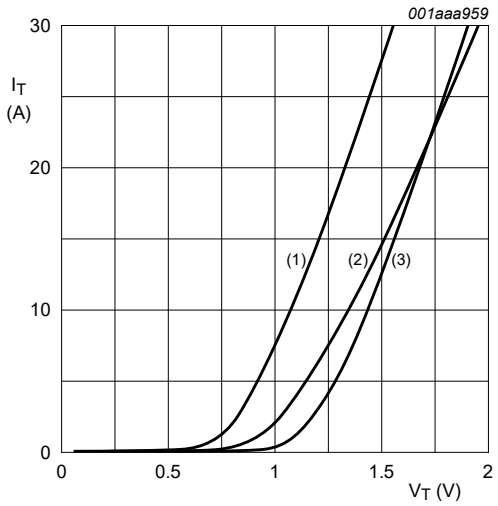


Fig. 9. Normalized holding current as a function of junction temperature



V_o = 1.06 V; R_s = 0.0304 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

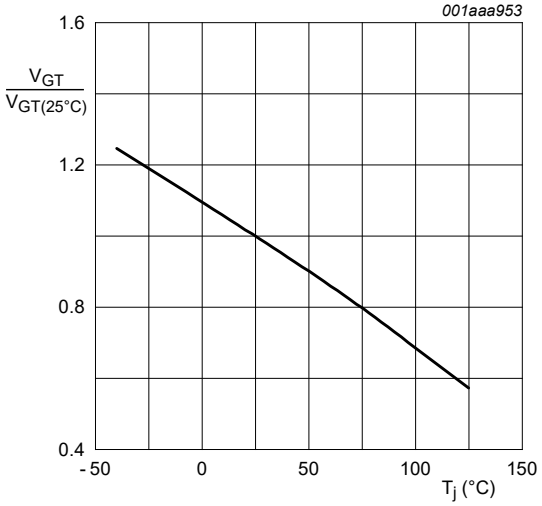
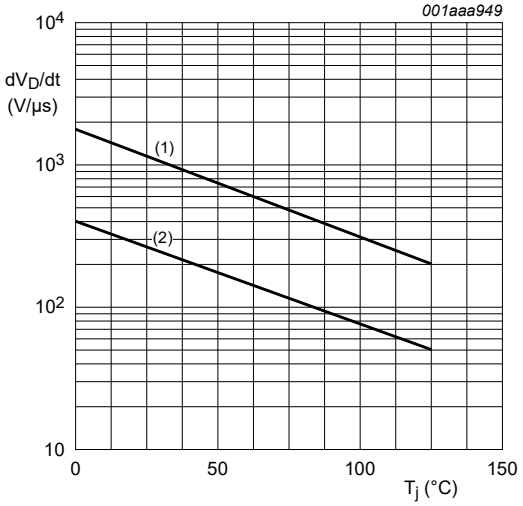


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

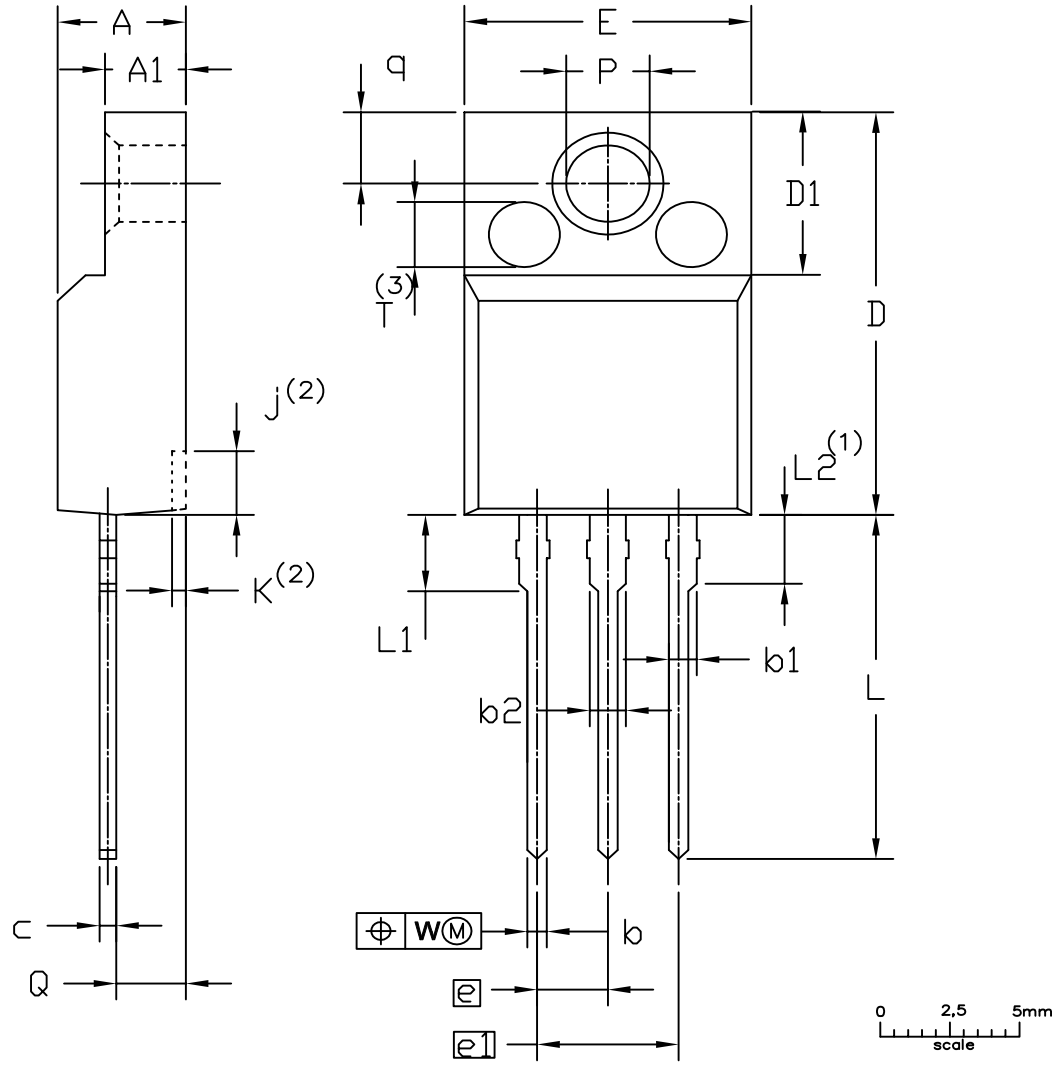


(1) R_{GK} = 100 Ω;
(2) gate open circuit

Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values

11. Package outline

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack" SOT186A



UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j(2)	K(2)	L	L_1	L_2(1) max.	P	Q	q	W	T(3)
mm	4.6	2.9	0.9	1.1	1.4	0.7	15.8	6.5	10.3	2.54	5.08	2.7	0.6	14.4	3.30	3	3.2	2.6	3.0	0.4	2.5
	4.0	2.5	0.7	0.9	1.0	0.4	15.2	6.3	9.7			1.7	0.4	13.5	2.79		3.0	2.3	2.6		

Notes
1. Terminal dimensions within this zone are uncotrolled
2. Dot lines area designs may vary
3. Eject pin mark is for reference only