GENERAL DESCRIPTION

Passivated thyristor in a plastic envelope, suitable for surface mounting, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. This thyristor has a high repetitive surge specification which makes it suitable for applications where high inrush currents or stall currents are likely to occur on a repetitive basis.

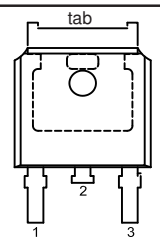
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	650	V
$I_{T(AV)}$	Average on-state current	7.5	A
$I_{T(RMS)}$	RMS on-state current	12	A
I_{TSM}	Non-repetitive peak on-state current	110	A
I_{TRM}	Repetitive peak on-state current	60	A

PINNING - SOT428

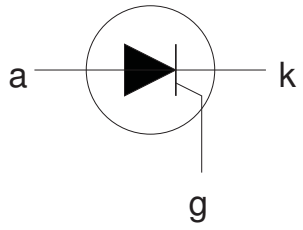
PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

PIN CONFIGURATION



DPAK (SOT428)

SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	half sine wave;	-	[1]650	V
$I_{T(AV)}$	Average on-state current	$T_{mb} \leq 103$ ˚C	-	7.5	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	12	A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; T_j = 25 ˚C prior to surge			
		t = 10 ms	-	110	A
		t = 8.3 ms	-	121	A
I_{TRM}	Repetitive peak on-state current	t = 10ms, τ = 3s, $T_{mb} \leq 45$˚C, no. of surges = 100k	-	60	A
I^2t	I^2t for fusing	t = 10 ms	-	61	A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	I_{TM} = 20 A; I_G = 50 mA; dI_G/dt = 50 mA/µs	-	50	A/µs
I_{GM}	Peak gate current		-	2	A
V_{GM}	Peak gate voltage		-	5	V
V_{RGM}	Peak reverse gate voltage		-	5	V
P_{GM}	Peak gate power		-	5	W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5	W
T_{stg}	Storage temperature		-40	150	˚C
T_j	Operating junction temperature		-	125	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.8	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb (FR4) mounted; footprint as in Fig.14	-	75	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A	-	2	15	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A	-	10	40	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	7	20	mA
V_T	On-state voltage	I_T = 23 A	-	1.4	1.75	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.6	1.5	V
		$V_D = V_{DRM(max)}$; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform;				
		Gate open circuit	50	130	-	V/µs
		R_{GK} = 100 Ω	200	1000	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 40 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 20 A; V_R = 25 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 50 V/µs; R_{GK} = 100 Ω	-	70	-	µs

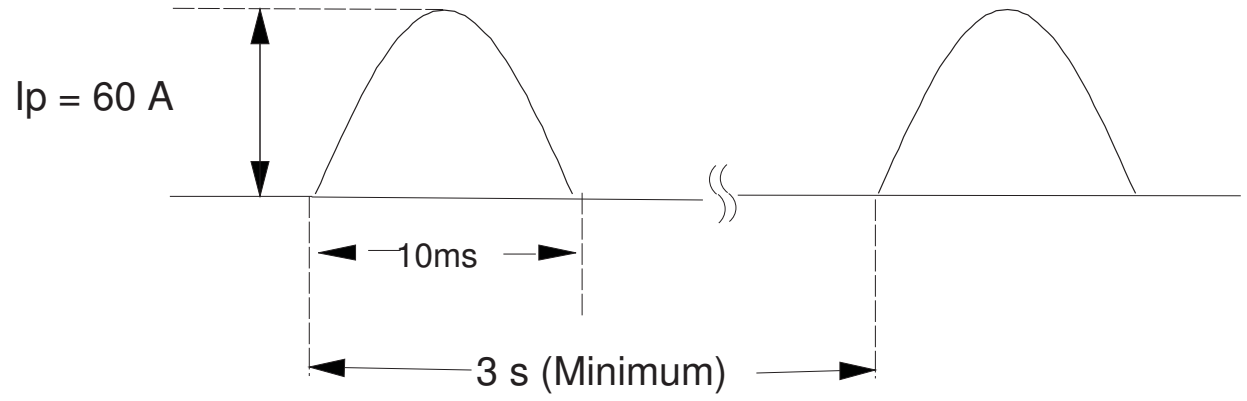


Fig.1. Repetitive surge conditions. I_P=60A (f=50Hz) at Tc=45˚C. Maximum number of cycles n=100k. Repetitive cycle T=3 seconds minimum.

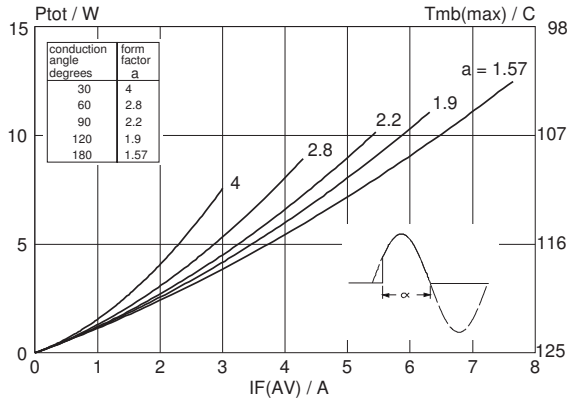


Fig.2. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.

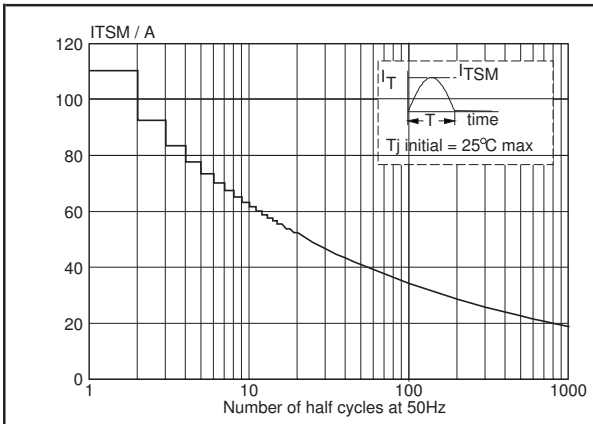


Fig.5. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

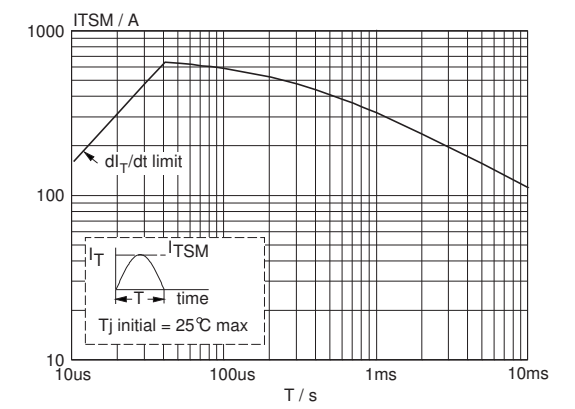


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

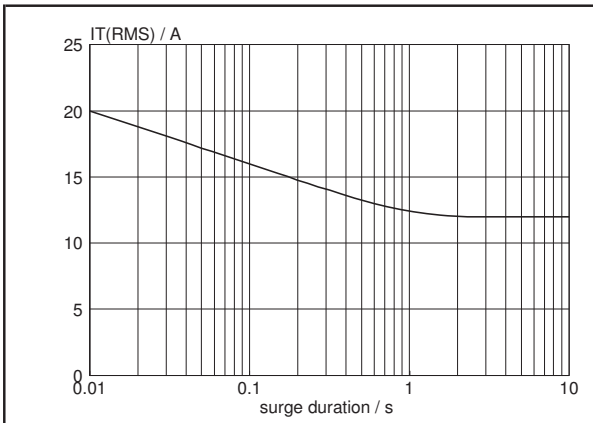


Fig.6. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 103^{\circ}C$.

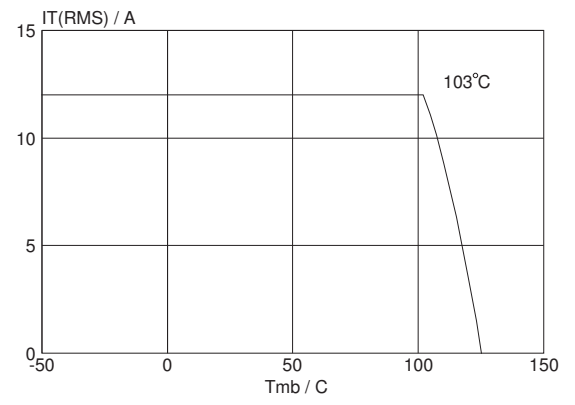


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

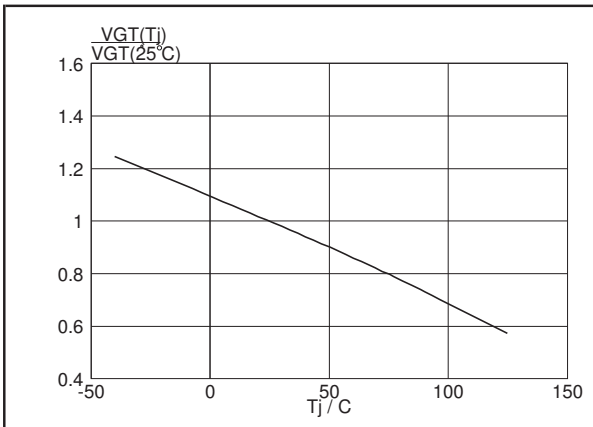


Fig.7. Normalised gate trigger voltage $V_{GT}(T_j)$/ $V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

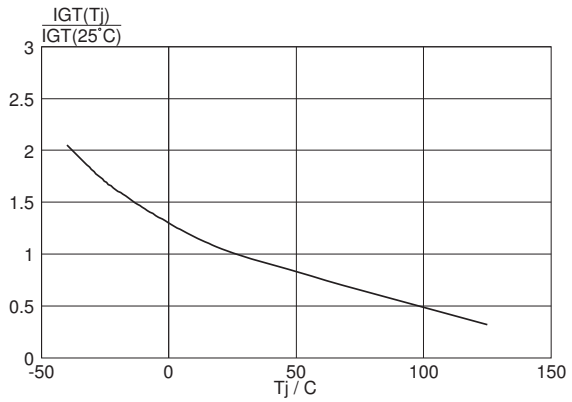


Fig.8. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

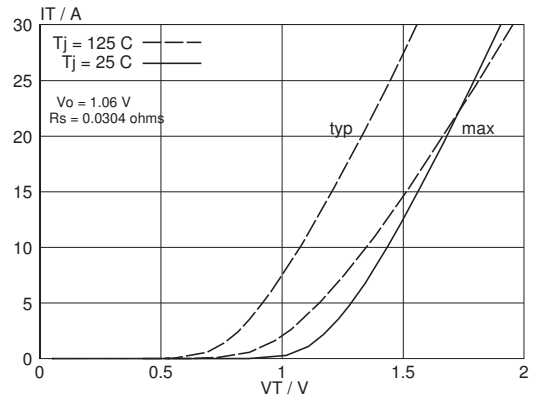


Fig.11. Typical and maximum on-state characteristic.

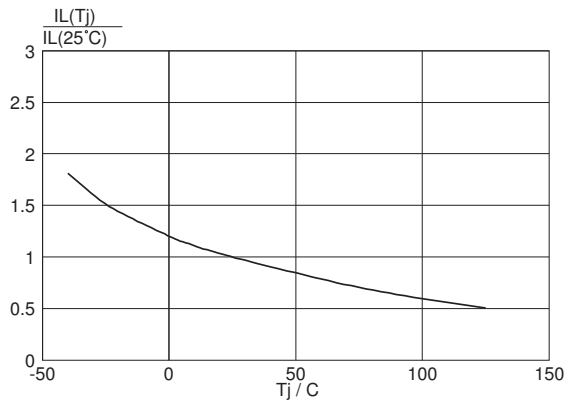


Fig.9. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

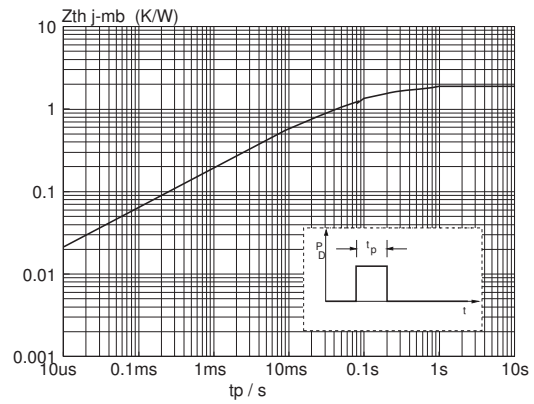


Fig.12. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

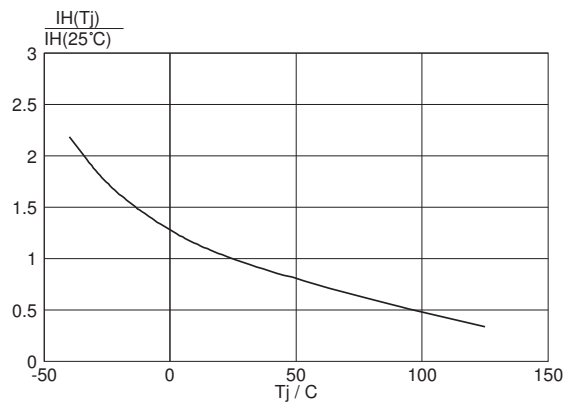


Fig.10. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

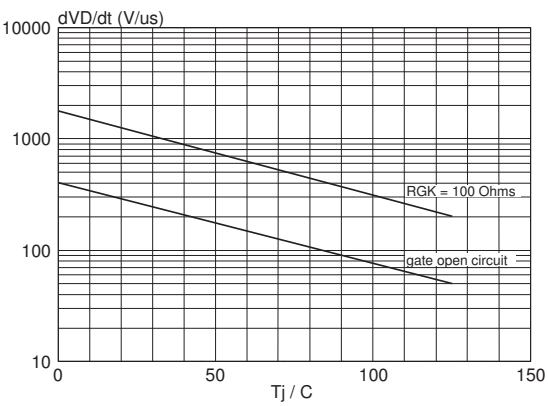
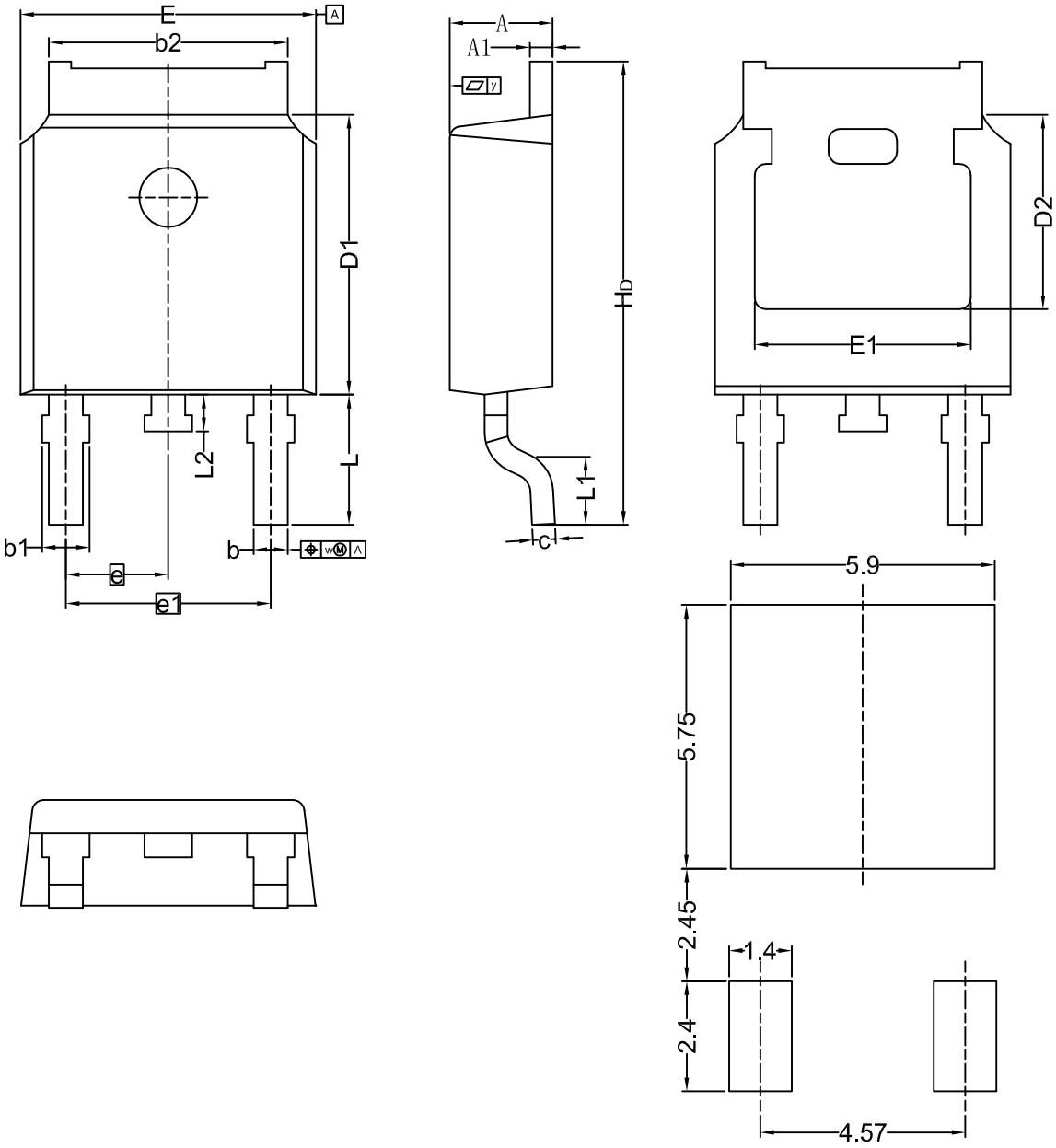


Fig.13. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

MECHANICAL DATA

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) TO252



Recommended Footprint

Unit	A	A1	b	b1	b2	c	D1	D2	E	E1	e	e1	H_D	L	L1	L2	w	y
min	2.22	0.46	0.71	0.72	5.00	0.20	5.98	4.00	6.47	4.45	2.285	4.57	9.60	2.90 (Ref.)	0.50	0.50	0.20	0.20
mm nom	2.38	0.93	0.89	1.10	5.46	0.56	6.22	---	6.73	---			10.40		---	0.90		
max																		

IMPORTANT NOTICE – PLEASE READ CAREFULLY

SZGKTMicroelectronics NV and its subsidiaries reserve the right to make changes, corrections, enhancements, modifications, and improvements toSZGKT.