## 1. General description

Planar passivated high commutation three quadrant triac in a SOT54 (TO-92) plastic package. This "series B" triac is designed to commutate the full RMS current at the maximum junction temperature without the aid of a snubber.

## 2. Features and benefits

- 3Q technology for improved noise immunity
- High commutation capability with maximum false trigger immunity
- High voltage capability
- Less sensitive gate for highest noise immunity
- Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

## 3. Applications

- General purpose motor control
- Small loads in washing machines
- Solenoid drivers

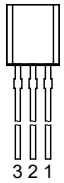
## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | - | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{lead} \leq$ 54 °C; Fig. 1; Fig. 2; Fig. 3 | | - | - | 1 | A |
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 7 | | 5 | - | 50 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 7 | | 5 | - | 50 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 7 | | 5 | - | 50 | mA |

## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | T2 | main terminal 2 |   TO-92 (SOT54) |   sym051 |
| 2 | G | gate | | |
| 3 | T1 | main terminal 1 | | |

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| T201-800B | TO-92 | plastic single-ended leaded (through hole) package; 3 leads | SOT54 |

## 7. Limiting values

**Table 4. Limiting values**

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{lead} \leq$ 54 °C; Fig. 1; Fig. 2; Fig. 3 | | - | 1 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 16.8 ms | | - | 13.7 | A |
| | | full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 20 ms; Fig. 4; Fig. 5 | | - | 12.5 | A |
| $I^2t$ | $I^2t$ for fusing | $t_p$ = 10 ms; SIN | | - | 0.78 | A²s |
| $dI_T/dt$ | rate of rise of on-state current | $I_G$ = 0.2 A | | - | 100 | A/µs |
| $I_{GM}$ | peak gate current | | | - | 2 | A |
| $P_{GM}$ | peak gate power | | | - | 5 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | | - | 0.1 | W |
| $T_j$ | junction temperature | | | -40 | 125 | °C |

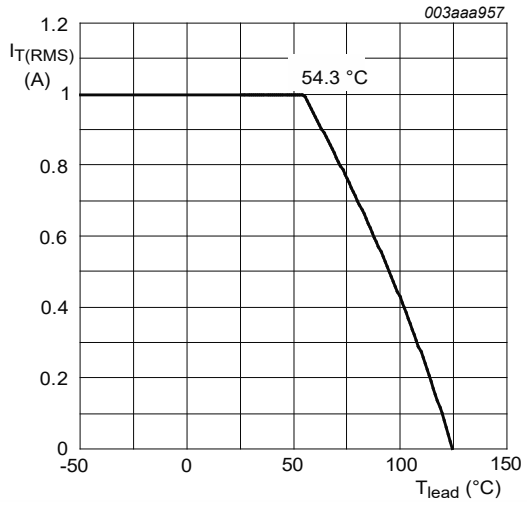
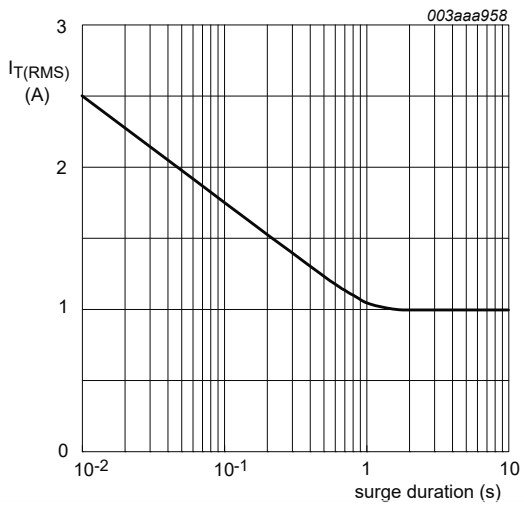
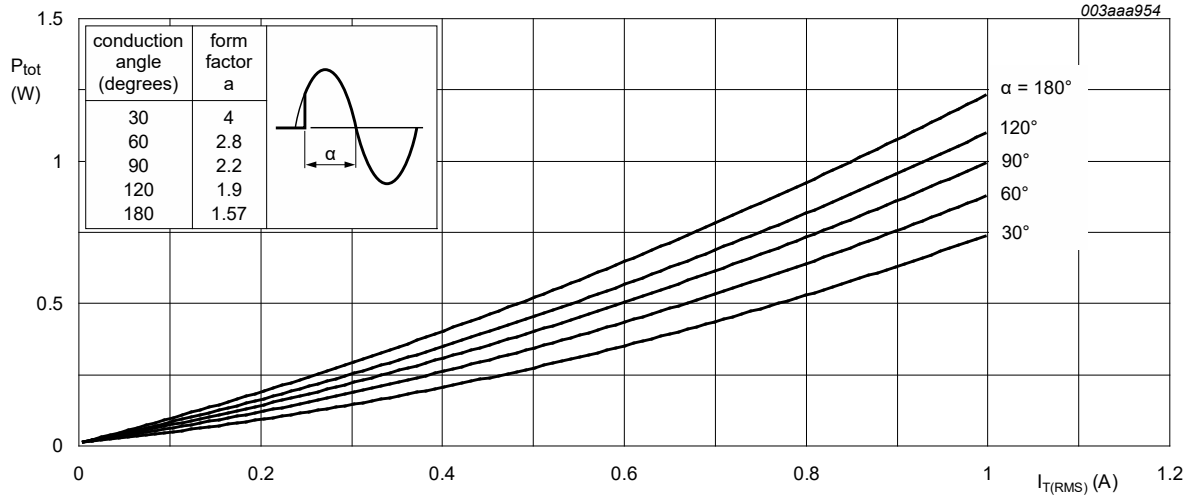



**Fig. 1. RMS on-state current as a function of lead temperature; maximum values**



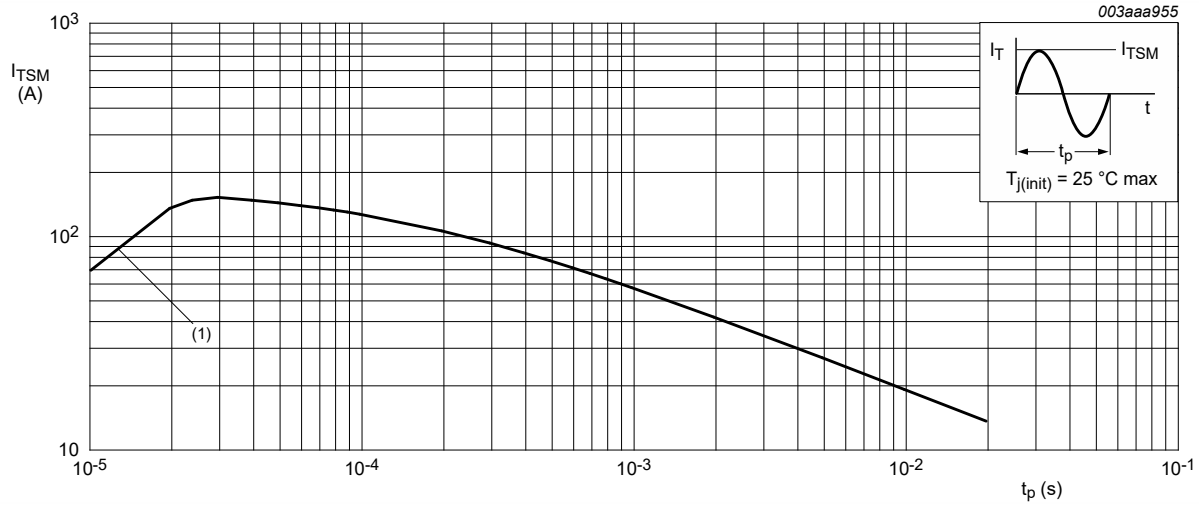

f = 50 Hz; $T_{lead}$ = 54 °C

**Fig. 2. RMS on-state current as a function of surge duration; maximum values**




α = conduction angle
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

**Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values**



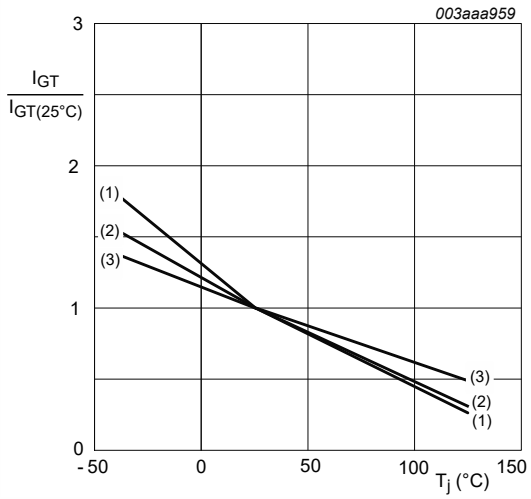

$t_p \leq 20$ ms
(1) $dI_T/dt$ limit

**Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values**

## 8. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 7 | | 5 | - | 50 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 7 | | 5 | - | 50 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 7 | | 5 | - | 50 | mA |
| $I_L$ | latching current | $V_D$ = 12 V; $I_G$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 8 | | - | - | 30 | mA |
| | | $V_D$ = 12 V; $I_G$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 8 | | - | - | 50 | mA |
| | | $V_D$ = 12 V; $I_G$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 8 | | - | - | 30 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $T_j$ = 25 °C; Fig. 9 | | - | - | 30 | mA |
| $V_T$ | on-state voltage | $I_T$ = 1.4 A; $T_j$ = 25 °C; Fig. 10 | | - | 1.2 | 1.5 | V |
| $V_{GT}$ | gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A; $T_j$ = 25 °C; Fig. 11 | | - | 0.7 | 1 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C; Fig. 11 | | 0.2 | 0.3 | - | V |
| $I_D$ | off-state current | $V_D$ = 800 V; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |
| **Dynamic characteristics** | | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 536 V; $T_j$ = 125 °C; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform; gate open circuit; Fig. 12 | | 1000 | - | - | V/µs |
| $dI_{com}/dt$ | rate of change of commutating current | $V_D$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 1 A; $dV_{com}/dt$ = 20 V/s; (snubberless condition); gate open circuit | | 12 | - | - | A/ms |
| | | $V_D$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 1 A; $dV_{com}/dt$ = 10 V/µs; gate open circuit | | 16 | - | - | A/ms |




(1) T2- G-
(2) T2+ G-
(3) T2+ G+

**Fig. 7. Normalized gate trigger current as a function of junction temperature**

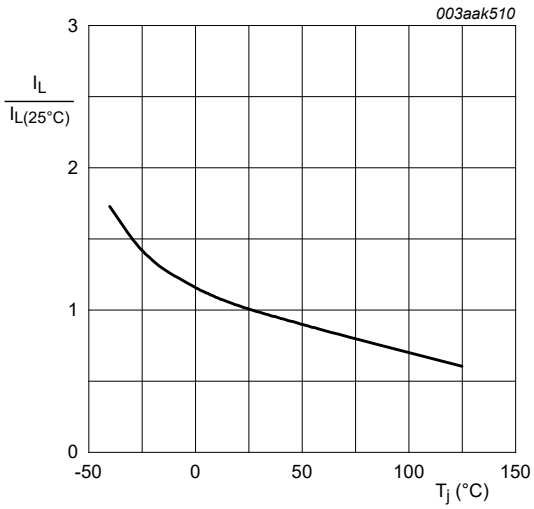



**Fig. 8. Normalized latching current as a function of junction temperature**

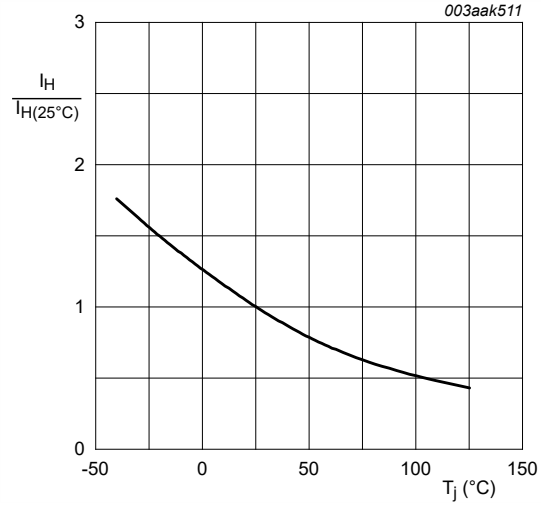
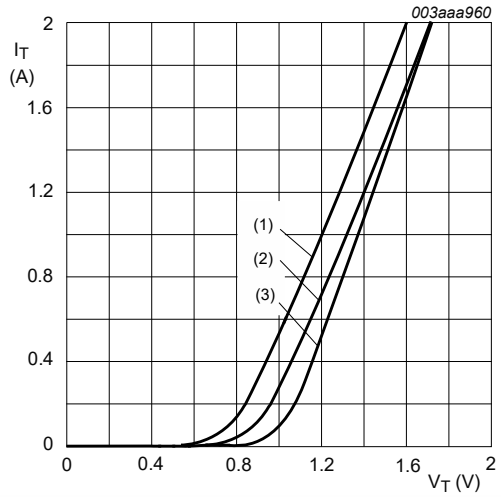



**Fig. 9. Normalized holding current as a function of junction temperature**




$V_o$ = 1.02 V; $R_s$ = 0.358 Ω
(1) $T_j$ = 125 °C; typical values
(2) $T_j$ = 125 °C; maximum values
(3) $T_j$ = 25 °C; maximum values

**Fig. 10. On-state current as a function of on-state voltage**

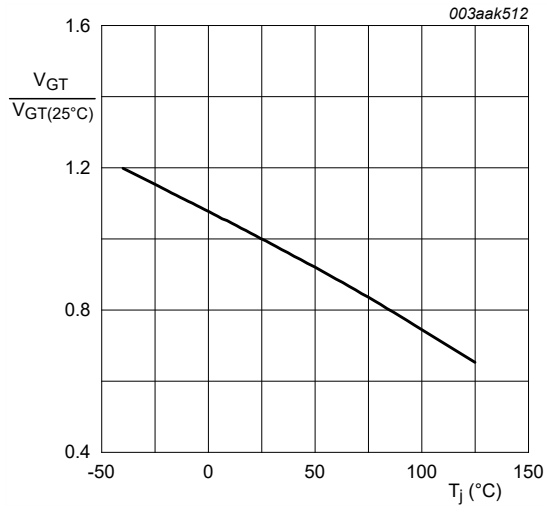



Fig. 11. Normalized gate trigger voltage as a function of junction temperature

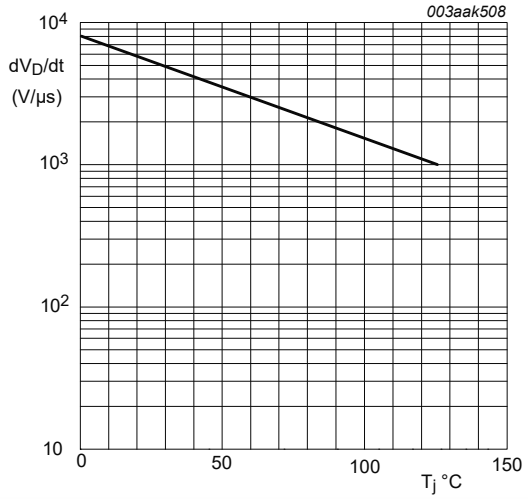



Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values

## 9. Package outline

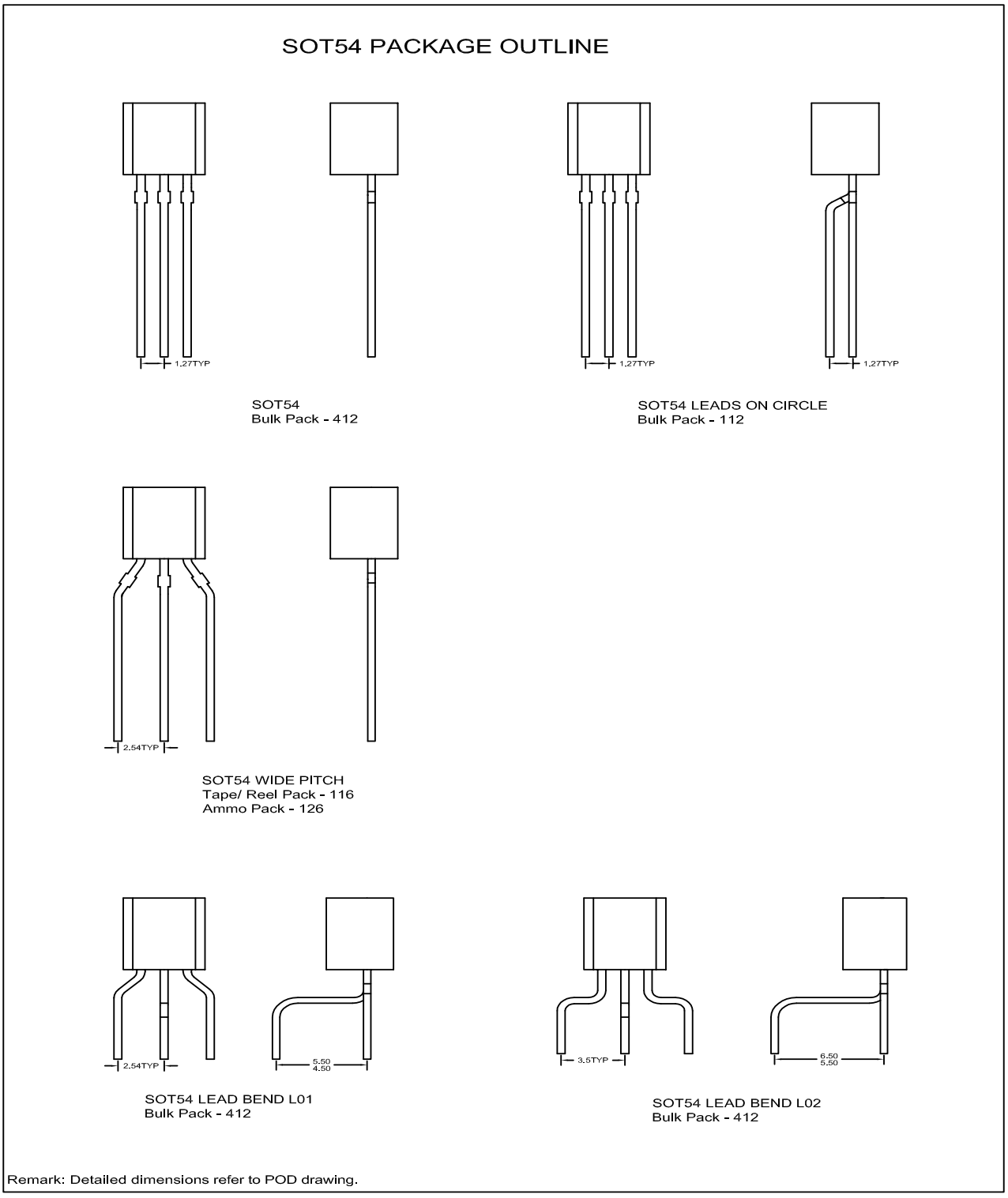



**Fig. 13. Package outline TO-92 (SOT54)**