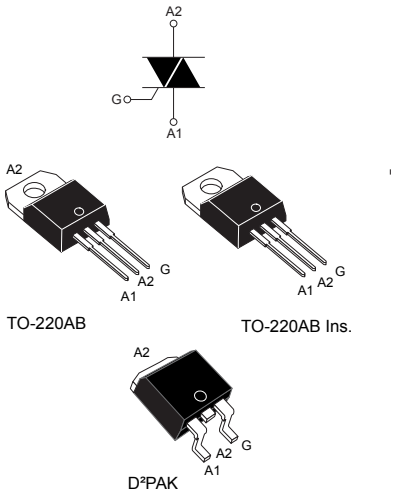
BTA12, BTB12, T1205
T1210, T1235, T1250

Datasheet

12 A Snubberless, logic level and standard Triacs



Features

- Medium current Triac
- Low thermal resistance with clip bonding
- Low thermal resistance insulation ceramic for insulated BTA
- High commutation (4Q) or very high commutation (3Q) capability
- Packages are RoHS (2011/65/EU) compliant

Description

Available either in through-hole or surface mount packages, the **B**TA12, **B**TB12 and T12xx Triac series are suitable for general purpose mains power AC switching. They can be used as ON/OFF function in applications such as static relays, heating regulation or induction motor starting circuit. They are also recommended for phase control operations in light dimmers and appliance motors speed controllers.

The Snubberless versions (W suffix and T12xx) are especially recommended for use on inductive loads, because of their high commutation performance. By using an internal ceramic pad, the Snubberless™ series provide an insulated tab (rated at 3500 V_{RMS}) .

Logic Level BTA12-600TW and BTA12-600SW offer low holding current, ideal to design light dimmers for LED lamps.

Figure 1. Ordering information scheme (BTA12 and BTB12 series)

BT B 12 - 600 BW RG

Triacseries

Insulation
A = insulated
B = non insulated

Current
12 = 12A

Voltage Sensitivity
600 = 600V 800
= 800V

and type
B = 50 mA standard
C = 25 mA standard
SW = 10 mA logic level
BW = 50 mA Snubberless
CW = 35 mA Snubberless
TW = 5 mA logic level

Packing mode RG = Tube

Figure 2. Ordering information scheme (T12 series)

T 12 35 - 600G (-TR)

Triac series

Current
12 = 12 A
Sensitiyity
50 = 50 mA
35 = 35 mA
10 = 10 mA
Voltage
600 or 6 = 600V
800 or 8 = 800V
Package
G=DPAK
Packing mode
Blank=Tube
-TR =Tape and reel

1 Characteristics

Table 1. Absolute maximum ratings (T_j = 25 °C unless otherwise stated)

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)	TO-220AB, D²PAK	T_c = 105 °C	12	A
		TO-220AB Ins.	T_c = 90 °C		
I_{TSM}	Non repetitive surge peak on-state current (full cycle, T_j initial = 25 °C)	f = 50 Hz	t = 20 ms	120	A
		f = 60 Hz	t_p = 16.7 ms	126	
I^2t	I^2t value for fusing		t_p = 10 ms	78	A^2s
dI/dt	Critical rate of rise of on-state current I_G = 2 x I_{GT}, tr ≤ 100 ns	f = 120 Hz	T_j = 125 °C	50	A/µs
V_{DSM}/V_{RSM}	Non repetitive surge peak off-state voltage	t_p = 10 ms	T_j = 25 °C	V_{DRM} / V_{RRM} + 100	V
I_{GM}	Peak gate current	t_p = 20 µs	T_j = 125 °C	4	A
$P_{G(AV)}$	Average gate power dissipation		T_j = 125 °C	1	W
T_{stg}	Storage junction temperature range			-40 to +150	°C
T_j	Operating junction temperature range			-40 to +125	°C

Table 2. Electrical characteristics (T_j = 25 °C, unless otherwise specified) - Snubberless™ and logic level (3 quadrants)

Symbol	Parameter	Quadrant		T1205 LTB12-TW LTA12-TW	T1210 LTB12-SW LTA12-SW	T1235 LTB12-CW LTA12-CW	T1250 LTB12-BW LTA12-BW	Unit
I_{GT} (1)	V_D = 12 V, R_L = 30 Ω	I - II - III	Max.	5	10	35	50	mA
V_{GT}		I - II - III	Max.	1.3				V
V_{GD}	V_D = V_{DRM}, R_L = 3.3 kΩ, T_j = 125 °C	I - II - III	Min.	0.2				V
I_H (2)	I_T = 100 mA	I - II - III	Max.	10	15	35	50	mA
I_L (2)	I_G = 1.2 x I_{GT}	I - III	Max.	10	25	50	70	mA
		II	Max.	15	30	60	80	
dV/dt (2)	V_D = 67% V_{DRM}, gate open, T_j = 125 °C		Max.	20	40	500	1000	V/µs
(dI/dt)c (2)	(dV/dt)c = 0.1 V/µs, T_j = 125 °C		Min.	3.5	6.5			A/ms
	(dV/dt)c = 10 V/µs, T_j = 125 °C		Min.	1.0	2.9			
	Without snubber, T_j = 125 °C		Min.			6.5	12	

1. *Minimum I_{GT} is guaranteed at 5 % of I_{GT} max.*
2. *For both polarities of A2 referenced to A1*

Table 3. Electrical characteristics (T_j = 25 °C, unless otherwise specified) - Standard Triac (4 quadrants)

Symbol	Parameter	Quadrant		Value		Unit
				C	B	
I_{GT} (1)	V_D = 12 V, R_L = 30 Ω	I - II - III	Max.	25	50	mA
		IV		50	100	
V_{GT}		All	Max.	1.3		V
V_{GD}	V_D = V_{DRM}, R_L = 33 kΩ, T_j = 125 °C	All	Min.	0.2		V
I_H (2)	I_T = 500 mA	I - II - III	Max.	25	50	mA
I_L	I_G = 1.2 I_{GT}	I - III - IV	Max.	40	50	mA
		II		80	100	
dV/dt (2)	V_D = 67 % V_{DRM} gate open, T_j = 125 °C		Min.	200	400	V/µs
(dV/dt)c (2)	(dI/dt)c = 5.3 A/ms, T_j = 125 °C		Min.	5	10	V/µs

1. *Minimum I_{GT} is guaranteed at 5 % of I_{GT} max.*
2. *For both polarities of A2 referenced to A1*

Table 4. Static electrical characteristics

Symbol	Test conditions			Value	Unit
V_{TM} (1)	I_{TM} = 17 A, t_p = 380 µs	T_j = 25 °C	Max.	1.55	V
V_{TO} (1)	threshold on-state voltage	T_j = 125 °C	Max.	0.85	V
R_D (1)	Dynamic resistance	T_j = 125 °C	Max.	35	mΩ
I_{DRM} I_{RRM}	V_{DRM} = V_{RRM}	T_j = 25 °C	Max.	5	µA
		T_j = 125 °C	Max.	1	mA

1. *For both polarities of A2 referenced to A1*

Table 5. Thermal resistance

Symbol	Parameter				Value	Unit
$R_{th(j-c)}$	Max. junction to case thermal resistance (AC)		D^2PAK / TO-220AB	Max.	1.4	°C/W
			TO-220AB insulated	Max.	2.3	
$R_{th(j-a)}$	Junction to ambient	S = 2 cm² (1)	D^2PAK	Typ.	45	°C/W
	Junction to ambient		TO-220AB / TO-220AB insulated	Typ.	60	

1. *S = Copper surface under tab.*

1.1 Characteristics (curves)

Figure 1. Maximum power dissipation versus on-state RMS current (full cycle)

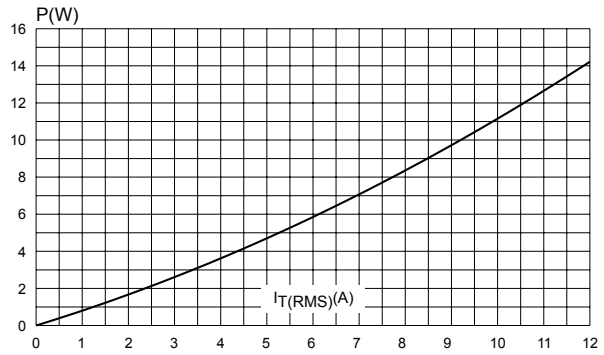


Figure 2. RMS on-state current versus case temperature (full cycle)

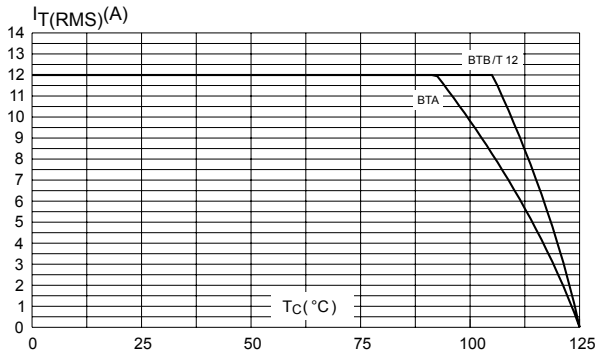


Figure 3. RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35 µm) (full cycle)

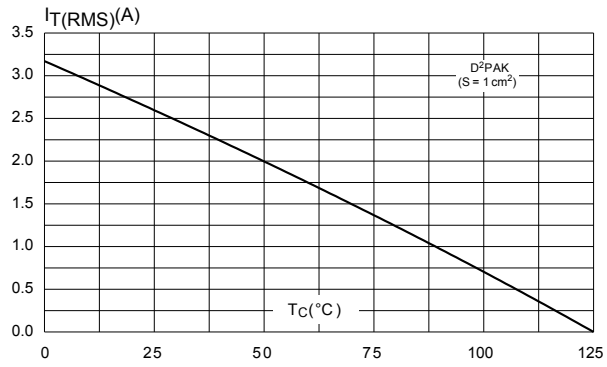


Figure 4. Relative variation of thermal impedance versus pulse duration

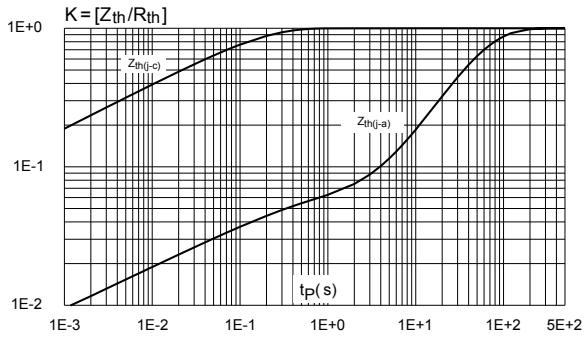


Figure 5. On-state characteristics (maximum values)

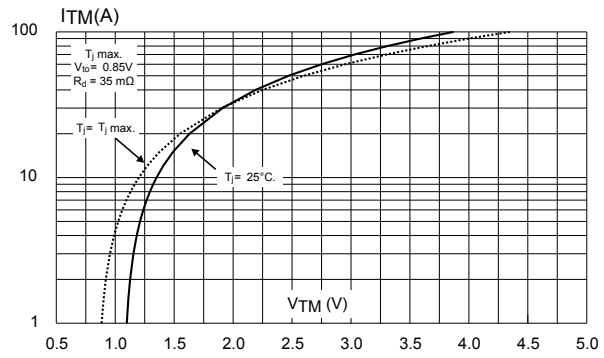


Figure 6. Surge peak on-state current versus number of cycles

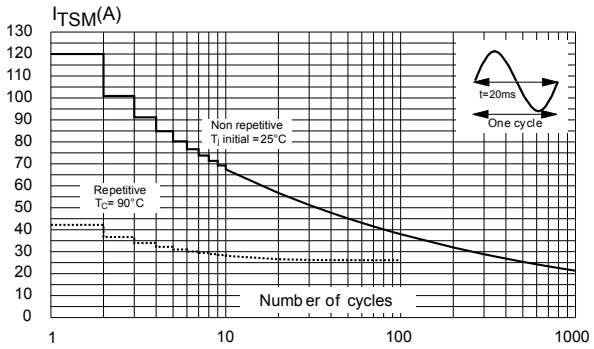


Figure 7. Non repetitive surge peak on-state current for a sinusoidal pulse

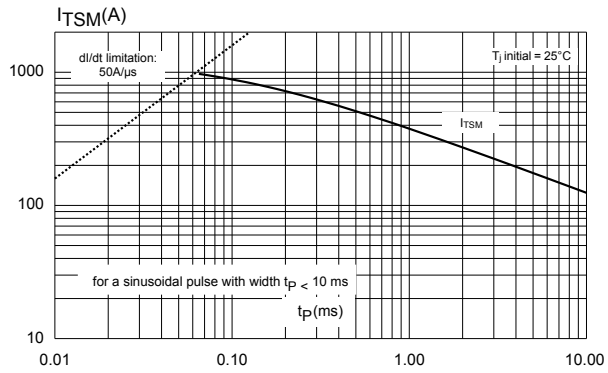


Figure 8. Relative variation of gate trigger current holding current and latching current versus junction temperature (typical values)

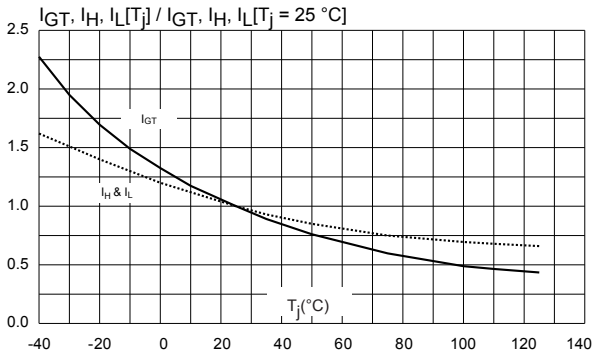


Figure 9. Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values)

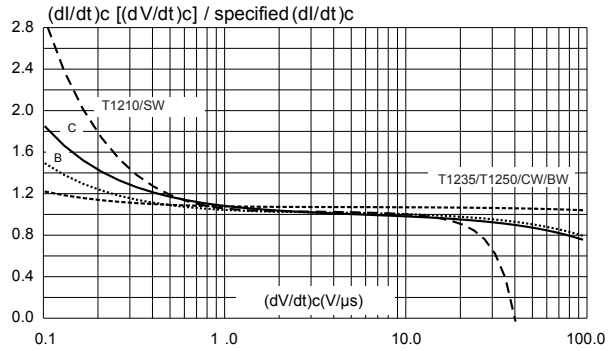


Figure 10. Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values)(TW)

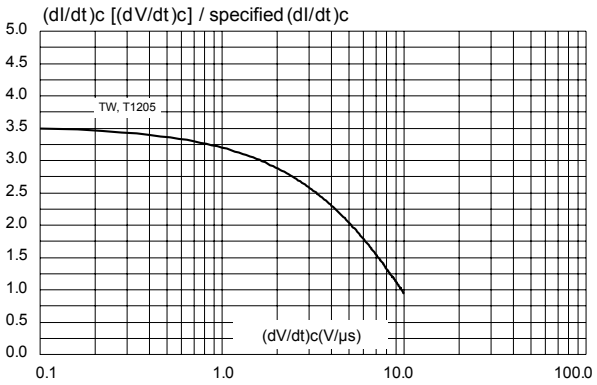


Figure 11. Relative variation of critical rate of decrease of main current versus junction temperature

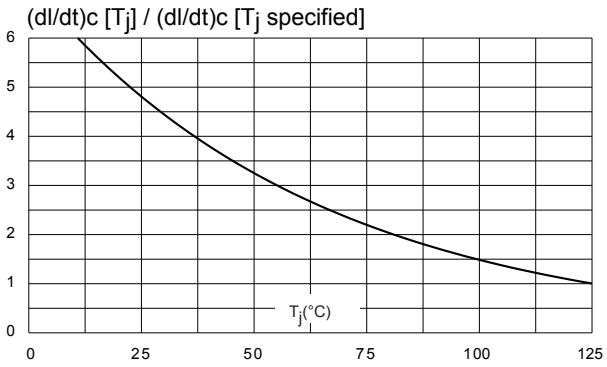
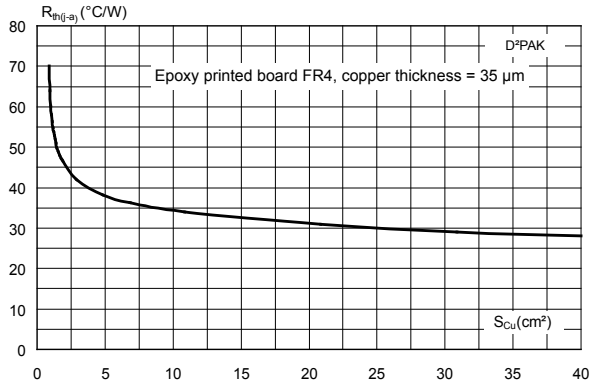


Figure 12. D^2PAK thermal resistance junction to ambient versus copper surface under tab

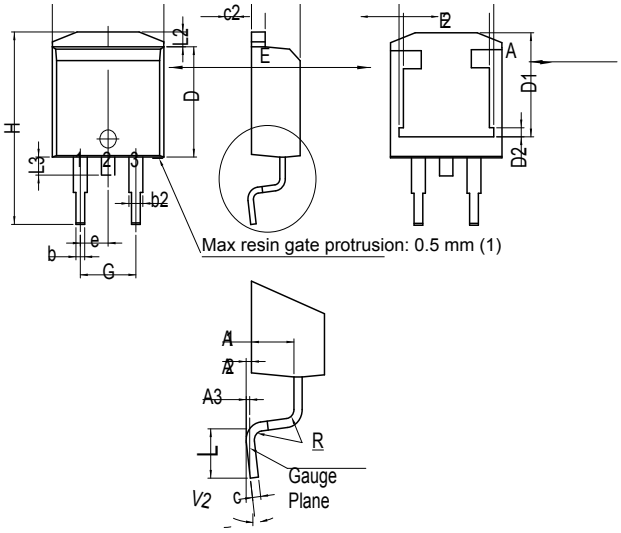


2 Package information

2.1 D²PAK package information

- ECOPACK2® compliant
- Lead-free package leads finishing
- Molding compound resin is halogen-free and meets UL standard level V0

Figure 13. D²PAK package outline



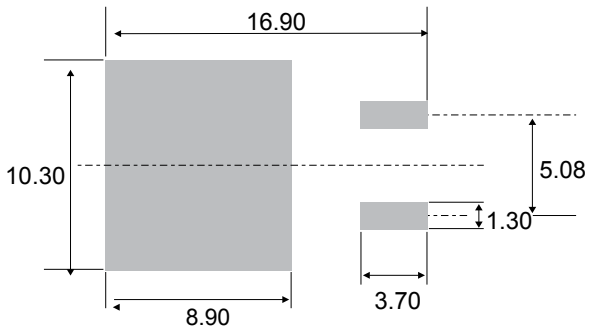
(1) Resin gate is accepted in each of position shown on the drawing, or their symmetrical.

Table 6. D²PAK package mechanical data

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.30		4.60	0.1693		0.1811
A1	2.49		2.69	0.0980		0.1059
A2	0.03		0.23	0.0012		0.0091
A3		0.25			0.0098	
b	0.70		0.93	0.0276		0.0366
b2	1.25		1.7	0.0492		0.0669
c	0.45		0.60	0.0177		0.0236
c2	1.21		1.36	0.0476		0.0535
D	8.95		9.35	0.3524		0.3681
D1	7.50		8.00	0.2953		0.3150
D2	1.30		1.70	0.0512		0.0669
e	2.54			0.1		
E	10.00		10.28	0.3937		0.4047
E1	8.30		8.70	0.3268		0.3425
E2	6.85		7.25	0.2697		0.2854
G	4.88		5.28	0.1921		0.2079
H	15		15.85	0.5906		0.6240
L	1.78		2.28	0.0701		0.0898
L2	1.27		1.40	0.0500		0.0551
L3	1.40		1.75	0.0551		0.0689
R		0.40			0.0157	
V2	0°		8°	0°		8°

1. *Dimensions in inches are given for reference only*

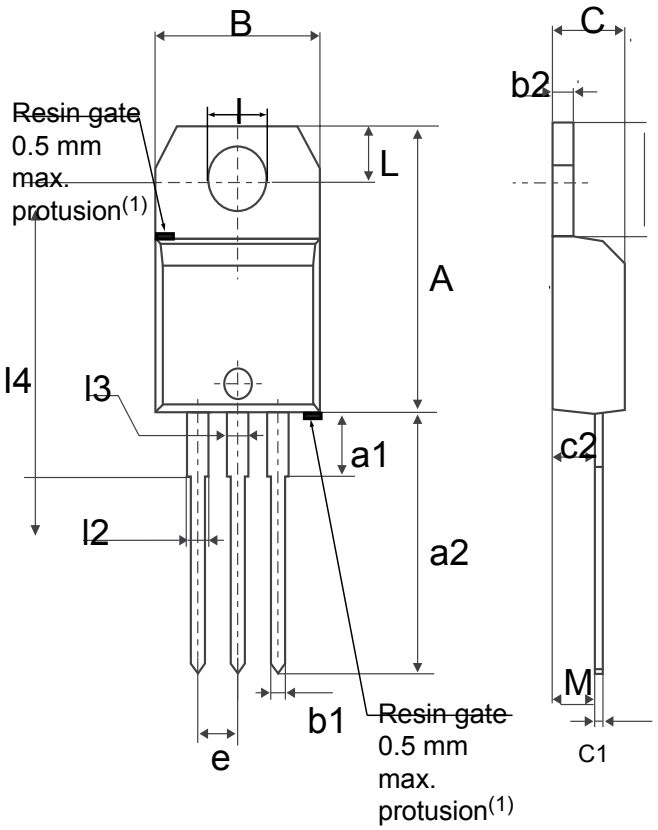
Figure 14. D²PAK recommended footprint (dimensions are in mm)



2.2 TO-220AB insulated package information

- Epoxy meets UL 94,V0
- Cooling method: by conduction (C)
- Recommended torque value: 0.55 N·m
- Maximum torque value: 0.70 N·m

Figure 15. TO-220AB insulated and non insulated package outline



Ref.	Dimensions					
	Millimeters			Inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	15.20		15.90	0.5984		0.6260
a1		3.75			0.1476	
a2	13.00		14.00	0.5118		0.5512
B	10.00		10.40	0.3937		0.4094
b1	0.61		0.88	0.0240		0.0346
b2	1.23		1.32	0.0484		0.0520
C	4.40		4.60	0.1732		0.1811
c1	0.49		0.70	0.0193		0.0276
c2	2.40		2.72	0.0945		0.1071
e	2.40		2.70	0.0945		0.1063
F	6.20		6.60	0.2441		0.2598
I	3.73		3.88	0.1469		0.1528
L	2.65		2.95	0.1043		0.1161
l2	1.14		1.70	0.0449		0.0669
l3	1.14		1.70	0.0449		0.0669
l4	15.80	16.40	16.80	0.6220	0.6457	0.6614
M		2.6			0.1024	

(1)Resin gate position accepted in one of the two positions or in the symmetrical opposites.